



PATENT ABSTRACTS OF JAPAN

(11) Publication number: **63211663 A**(43) Date of publication of application: **02.09.88**

(51) Int. Cl. **H01L 25/08**
H01L 23/52
H01R 9/09

(21) Application number: **62046007**(71) Applicant: **MITSUBISHI ELECTRIC CORP**(22) Date of filing: **26.02.87**(72) Inventor: **TANAKA HIROSHI****(54) CIRCUIT BOARD****(57) Abstract:**

PURPOSE: To realize a small-sized and thin semiconductor chip component packaged at a higher density and to reduce a space occupied by a related device or the like, by arranging semiconductor chips in parallel with each other, the semiconductor chips being layered semiconductor chips joined with each other with an adhesive material at their corresponding faces, and by arranging these layered semiconductor chips on an insulating substrate.

CONSTITUTION: A substrate region including first, second and third semiconductor chips 15, 16 and 17, an adhesive material 6a, a bump electrode 12a a conductive adhesive material 14a, substrate electrodes 5a and 5c and wires 7a and 7c is covered with a sealing material 8a. Thus, a first layered semiconductor chip structure is provided on one principal face of an insulating substrate 4. On the other face of the substrate, a second layered semiconductor chip structure consisting of a fourth semiconductor chip 16 providing the first layer and a fifth semiconductor chip 19 providing the second layer is arranged symmetrically with respect to the first layered semiconductor chip structure. The electrodes are interconnected and the structure is sealed with a sealing material 8b. In this manner, it is possible to realize a thin and small-sized semiconductor chip component having a higher density.

COPYRIGHT: (C)1988,JPO&Japio

